



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Stephen M. Watts

Art Unit: TBD

Serial No.: 10/026,085

Examiner: TBD

Filing Date: 12/21/01

Docket No.: TI-29923

Title: PARALLEL INTEGRATED CIRCUIT TEST APPARATUS AND TEST METHOD

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RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Assistant Commissioner for Patents
Washington, DC 20231

Attn: Customer Service Center
Initial Patent Examination Division

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)
I hereby certify that this correspondence is being
deposited with the United States Postal Service as first
class mail in an envelope addressed to: Assistant
Commissioner for Patents, Washington, DC 20231.

Marianna Smith 2-21-02
Marianna Smith Date

Dear Sir:

In response to the Notice to File Corrected Application Papers dated 01/28/02,
submitted herewith are five sheets of formal drawings in compliance with 37 CFR 1.84.

Respectfully submitted,

Jacqueline J. Garner
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